

II. REMARKS

Claims 1-20 are pending and are rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Morioka et al., (U.S. Patent No. 6,611,728) in view of Shimono (U.S. Patent No. 6,308,293). Claim 1 is also rejected under 35 U.S.C. § 101. Applicant traverses these rejections for the reasons stated below. Applicant does not acquiesce in the correctness of the rejections and reserves the right to present specific arguments regarding any rejected claims not specifically addressed. Further, Applicant reserves the right to pursue the full scope of the subject matter of the claims in a subsequent patent application that claims priority to the instant application.

Applicant respectfully submits that all claims are allowable over the cited art. "To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 706.02(j).

The grounds of rejection allege that Morioka et al. substantially teaches "a fault isolation system that compares faulty device features with the previously studied features listed in the defect table in order to identify causes of fail[ure] (e.g., col. 9, lines 9-30 & col. 11, lines 17-34)." The grounds of rejection admit that Morioka et al. "fails to explicitly teach inputting *suspected* faulty device features and comparing *suspected* faulty device features with previously studied features." As such, the grounds of rejection rely on Shimono as teaching a *suspected* feature comparison, citing col. 12, lines 38-65.

Yet, as respectfully submitted in the December 6, 2007 Amendment, the Morioka et al. defect location history list 111 is not used as a comparison with inputted defect data, but is instead is a collection of inspection data for each of a plurality of wafers being tested. Ultimately, the defect location history list 111 is analyzed to understand “how much defects caused by each process affect the yield.” (see, e.g., column 17, line 38.) Defect location history list’s 111 purpose is not for comparison with inputted defect data, as is claimed in the present application. Since defect location history list 111 is not used for comparison purposes in any manner in the Morioka et al. process, Applicant respectfully submits that the comparison feature is not taught by Morioka et al., and as such, there would be no motivation to incorporate an alleged *suspected* comparison feature of the Shimono process into the Morioka et al. process. Furthermore, there is no suggestion that the defect location history list 111 of Morioka et al. is compared with defect data *"in order to identify causes of the failure."*

Nor, would this feature be taught by Shimono. In Shimono, the suspected fault list 14 is derived from the circuit description of the LSI and test pattern 12 (see col. 8, lines 6-10) - not compared to the test pattern 12. Rather, the suspected fault list 14 is used to identify suspected circuit faults on which to perform a fault simulation (see col. 10, lines 7-19). As such, the comparison feature of claim 1 is also not taught by Shimono.

For these reasons, Applicant submits that claim 1 (and similarly claims 9, 15 and 18) are not obvious in view of the cited references. Each of the claims not specifically addressed herein is believed allowable for the reasons stated above, as well as their own unique features.

With respect to the 35 U.S.C. § 101 rejection of claim 1, the grounds of rejection allege that paragraph [0022] describes the claimed system as software *per se*, which is non-statutory. Applicant notes that this section of the present specification teaches quite the opposite.

Paragraph [0022] states "it is understood that the systems, functions, mechanisms, methods, engines and modules described herein *can be implemented in hardware, software, or a combination of hardware and software.*" In no manner does the specification limit the claimed system to software *per se*. As such, Applicant respectfully requests that the 35 U.S.C. § 101 be withdrawn.

Should the Examiner not issue a Notice of Allowance in view of the lack of disclosure of Morioka et al. and Shimono with regards to claimed features of the present invention, the Examiner is respectfully requested to specifically define the "inputted set of suspected faulty device features", and the "previously studied features" of Shimono in a non-final Office Action.

Applicant respectfully submits that the application is in condition for allowance. If the Examiner believes that anything further is necessary to place the application in condition for allowance, the Examiner is requested to contact Applicant's undersigned representative at the telephone number listed below.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Michael Hoffman", with a horizontal line extending to the right.

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